



HARDWARE DESCRIPTION OF DIGITAL HOPFIELD NEURAL NETWORKS FOR SOLVING SHORTEST PATH PROBLEM

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Abstract: The shortest path problem is an important issue in communication networks which is used by many practical routing protocols. The aim of this paper is to present an intelligent model based on Hopfield neural networks (HNNs) for solving shortest path problem and implement that on Field Programmable Gate Arrays (FPGAs) chips. The Cyclone II-EP2C70F896C6 FPGA chip from ALTERA Inc. is considered for hardware implementing and VHDL language is employed for hardware description. The synthesizing results show the proposed architecture of neuron is more efficient than relevant neuron model for chip area utilization and consequently improving the maximum operating frequency and power consumption. The proposed router core is employed to find shortest paths in ring, star and mesh communication networks and the results demonstrate the efficiency and superiority of proposed core.

Key words: *Hopfield neural network, shortest path problem, FPGA implementation, VHDL*

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1. Introduction

The key responsibility of the network layer in communication networks is the routing problem [1,2] which is considered as establishing paths from source nodes to destination nodes in connecting demand matrix for different applications. There are different metrics which are considered as the objective of routing protocols and have important effects on the network performance and quality of service. The most common used metric in routing protocols is the shortest-path attempting to find the paths with minimum length. The main idea behind this metric is that using the shortest-path will result in low end-to-end delays and low resource consumptions [3].

The routing problem is a complex and multi-constraint problem which is considered as a NP-hard problem. Therefore intelligent and meta-heuristic optimization

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